IN THE CLAIMS

Please amend claims 26 and 27 as set forth below.

1. - 25. (Canceled)

26. (Currently Amended) A semiconductor integrated circuit comprising:

a memory cell;

a first data line coupled to an output node of said memory cell;

a second data line paired with said first data line; and

a precharge circuit for precharging said first data line to a first final precharge potential and precharging said second data line to a second final precharge potential different from said first final precharge potential, such that when the memory cell is selected, the voltage potential of said first data line is at said first final precharge potential and the voltage potential of said second data line is at said second final precharge potential.

27. (Currently Amended) The semiconductor integrated circuit according to claim 26, further comprising:

a sense amplifier amplifying information stored in said memory cell to either a first potential or second potential,

wherein said first final precharge potential is equal to said second potential, and

wherein said second final precharge potential is between said first and second potentials.

28. (Previously Presented) The semiconductor integrated circuit according to claim 27,

wherein said sense amplifier has a first input node to receive said information outputted from said first data line, and a second input node to receive said second potential from said second data line as a reference potential.

29. (Previously Presented) The semiconductor integrated circuit according to claim 26,

wherein said memory cell has three transistors and has a second input node coupled to said second data line to receive an information signal.